Electric-Field Induced F^- Migration in Self-Aligned InGaAs MOSFETs and Mitigation

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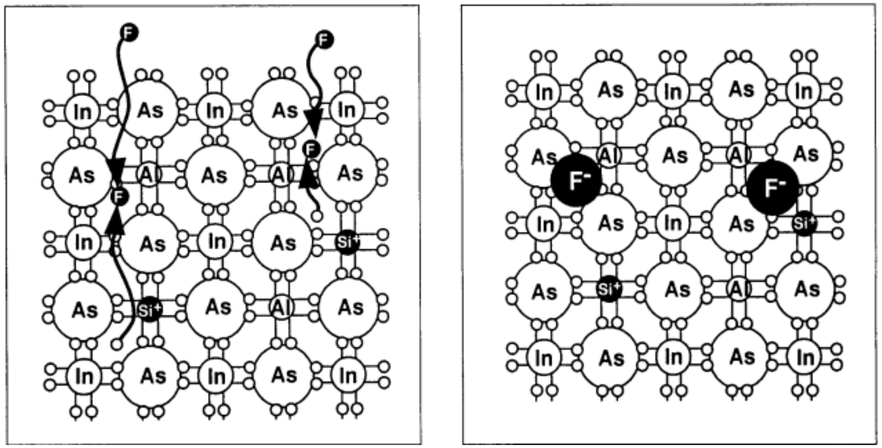
Acknowledgement: MTL and SEBL

Outline

- **Background: F in III-V's**
- **F-Induced Instability in InGaAs MOSFETs**
- **Independent confirmation of F role**
- **Mitigation**
- **Conclusions**

F-Induced Donor Passivation

- F known to migrate to Si:InAlAs, and passivate Si donors



Y. Yamamoto et al,
J. Electron. Mat. 1996

$F_{atmosphere}$ ----------> $F_{adsorbed}$

$F_{adsorbed}$ ----------> $F_{interstitial}$

$F_{interstitial} + e^-$ ----------> $F^-_{interstitial}$

$F^-_{interstitial} + D^+$ ----------> $F^- \text{-} D^+$

N. Hayafuji et al,
Mat. Res. Soc. Symp. Proc. 1996

F-Si complex observed

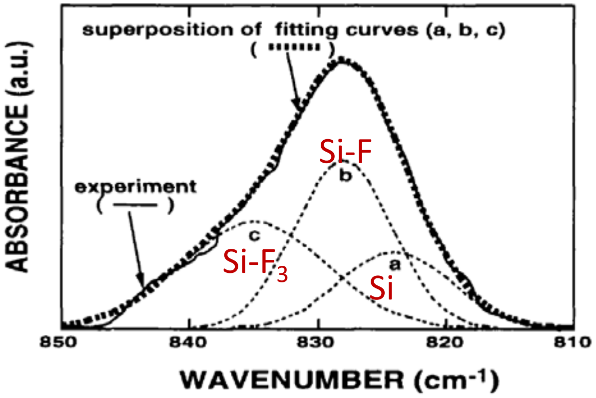
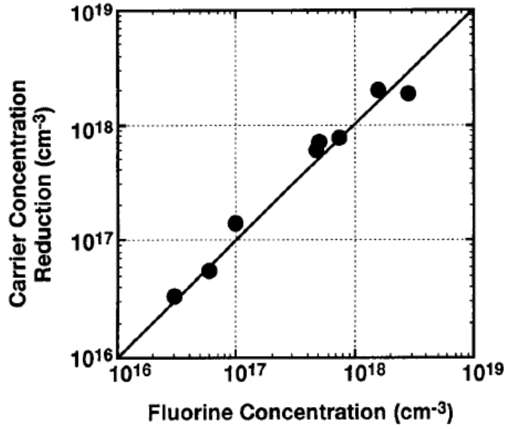


Figure 7. Gaussian curve fitting results for FTIR spectrum for Si-doped $Al_{0.48}In_{0.52}As$ layer after annealing.

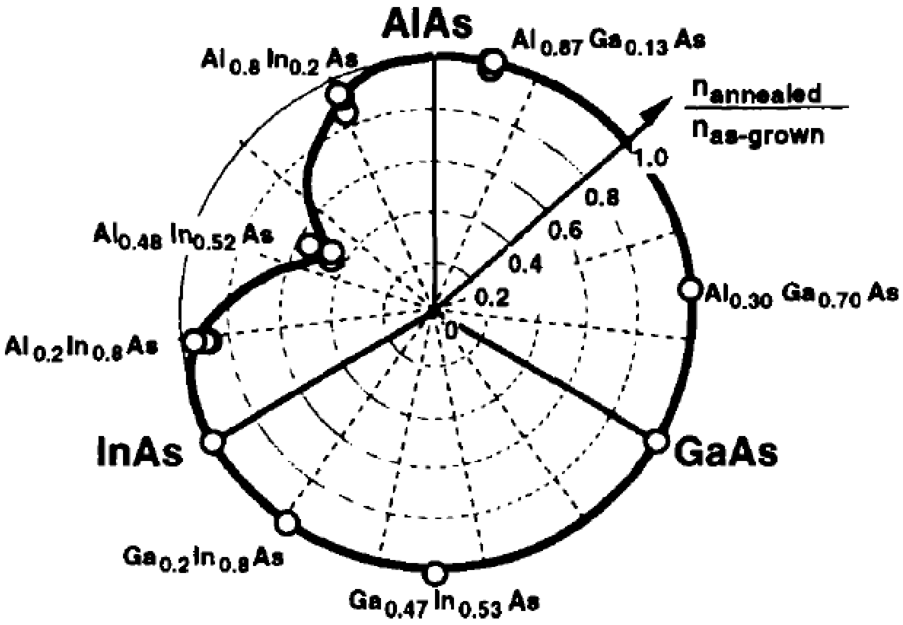
N. Hayafuji et al,
Mat. Res. Soc.
Symp. Proc. 1996

Electron concentration ↓

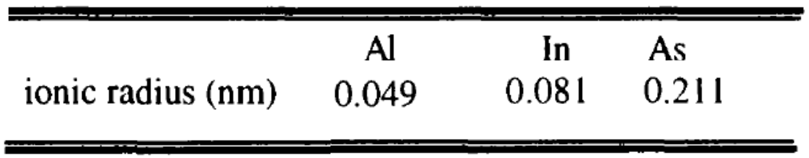


Selective F passivation

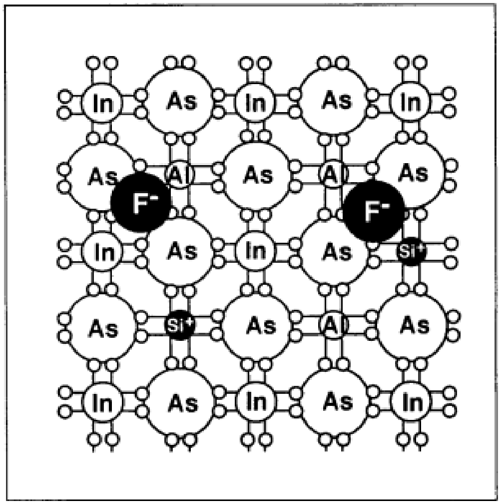
- F only affects n-InAlAs, but not InP or InGaAs



N. Hayafuji et al,
Mat. Res. Soc. Symp. Proc. 1996



	Al	In	As
ionic radius (nm)	0.049	0.081	0.211

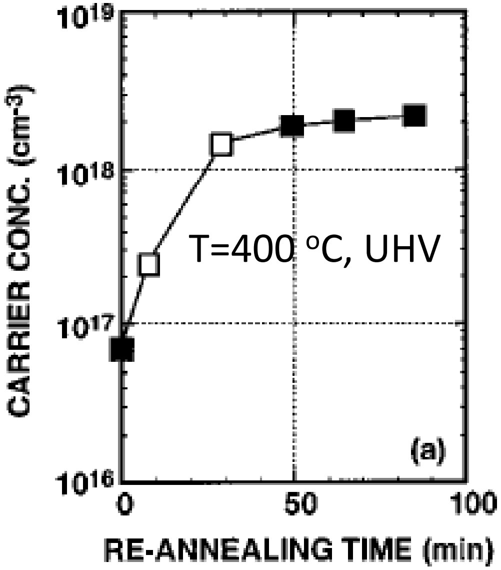


- InAlAs has strong tendency of ionization
- AlAs:InAs=1:1 gives the most localization of F due to ionic radius difference between Al and In

F-Induced Instability

- F-donor complex weakly bound

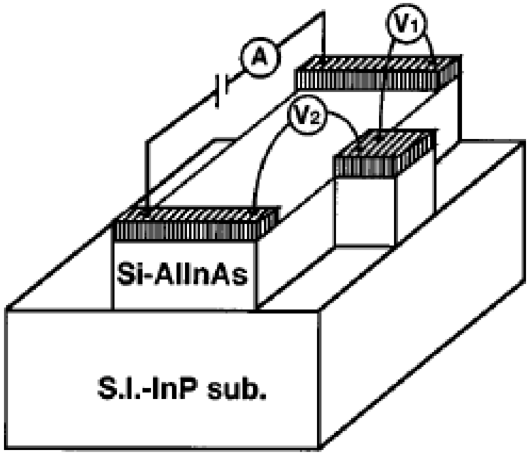
Thermal annealing

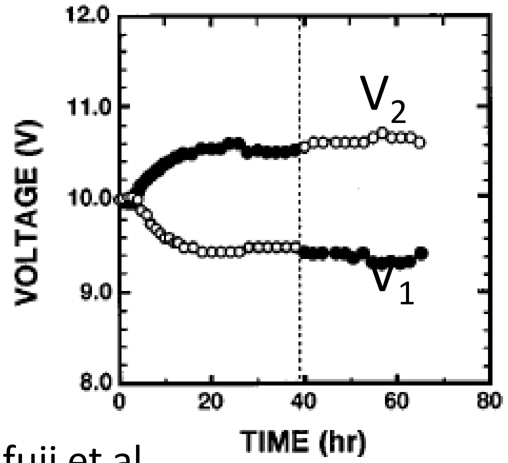


T=400 °C, UHV

N. Hayafuji et al, APL 1995

Electric field





N. Hayafuji et al, APL 1996

- Under high temperature or electric field, F^- bound to Si in InAlAs can easily dissociate and migrate

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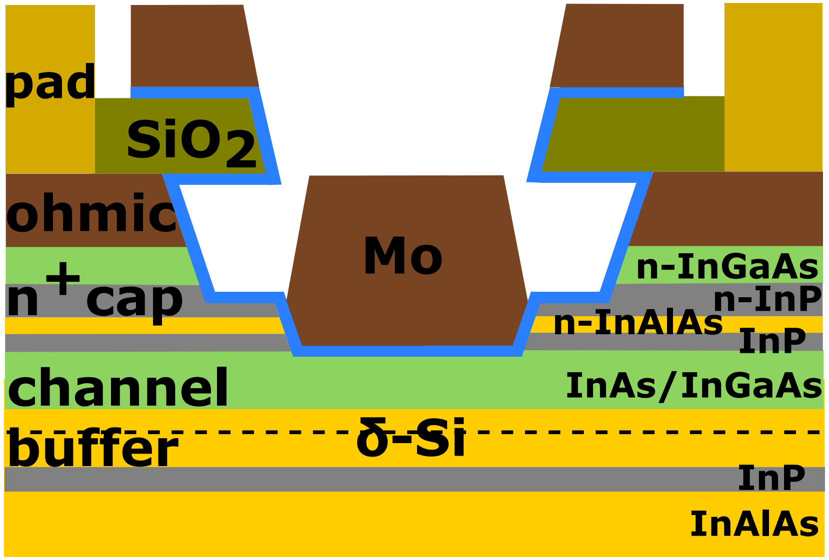
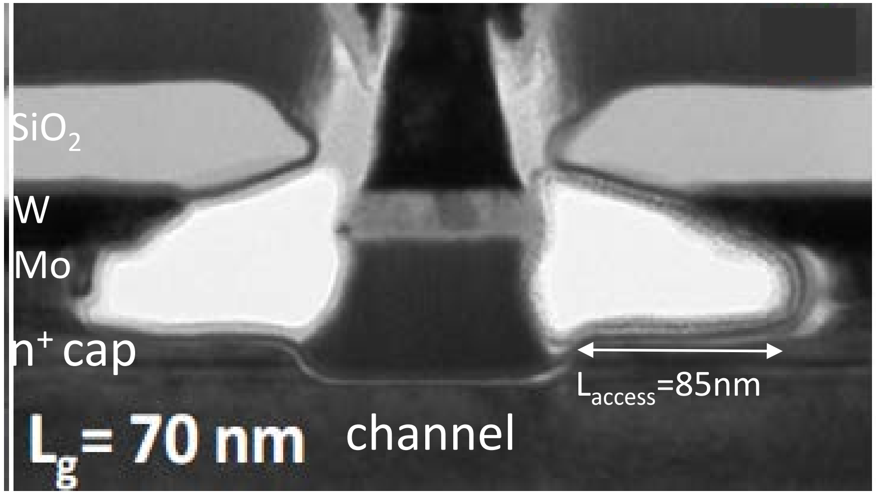
- **F-Induced Instability in InGaAs MOSFETs**
- Independent confirmation of F role
- Mitigation
- Conclusions

Self-aligned InGaAs MOSFETs



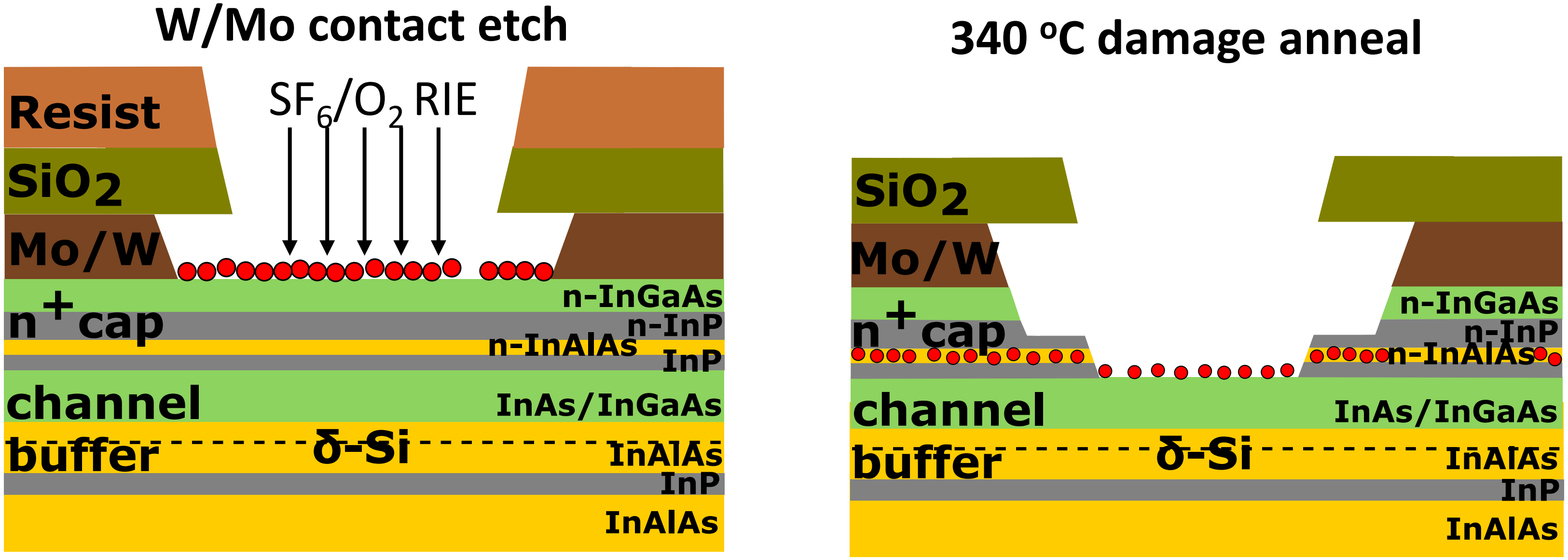


J. Lin et al, IEDM 2013

- Gate dielectric: 2.5 nm HfO_2
- Intrinsic channel: $In_{0.7}Ga_{0.3}As$/InAs/$In_{0.7}Ga_{0.3}As$ (1/2/5 nm)
- Composite n^+ cap: n-InGaAs/n-InP/n-InAlAs/i-InP
- Access region length: 85 nm

F in self-aligned InGaAs MOSFETs

- Si:InAlAs used in cap and access regions
- Process involves F-based RIE + thermal annealing

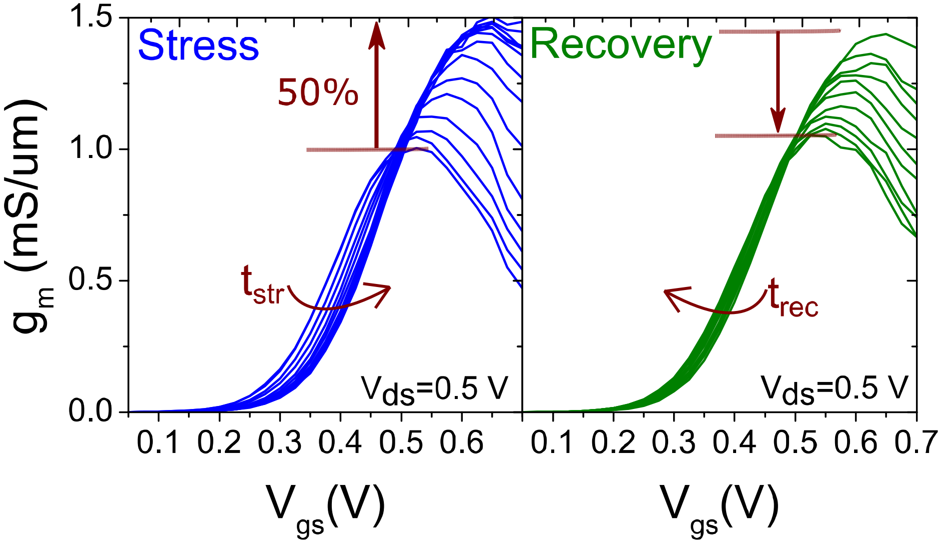


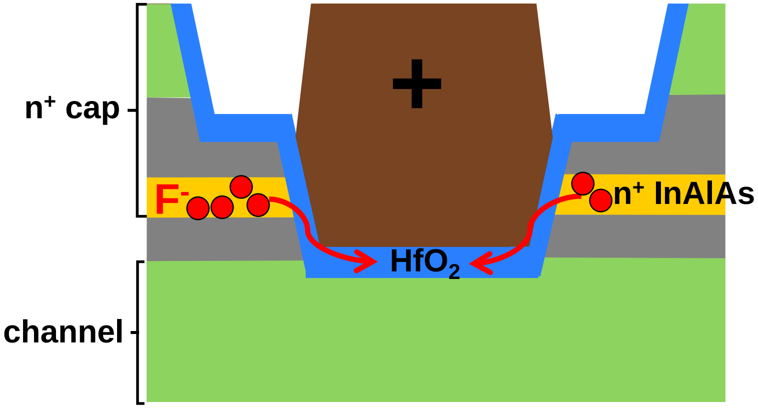
- F expected to concentrate under gate and in access regions
- Consequences:
  - $n_s\downarrow$, $R_{on}\uparrow$, $g_m\downarrow$ in virgin device
  - Reduced current drive
  - Device instability due to F migration

J. Lin et al, IEDM 2013

Forward Gate Stress

- Stress: $V_{gt} = V_{gs} - V_t = 0.8$ V, $V_{ds} = 0$ V, 1.5 h, at RT
- Recovery: $V_{gs} = 0$ V, $V_{ds} = 0$ V, 1 h, at RT





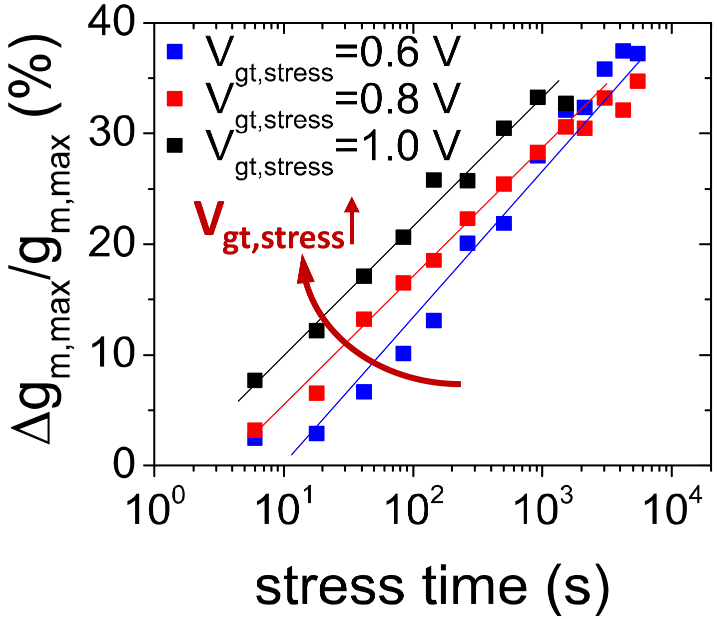
Positive gate voltage stress
($V_{gt} > 0$ V, $V_{ds} = 0$ V)

- During stress, F^- drifts from access regions into gate oxide, reactivating Si dopants in n-InAlAs in access region
  - ➢ $n_s \uparrow$, $R_{on} \downarrow$ and $g_m \uparrow$
- During recovery, F^- diffuses back to n-InAlAs and passivates Si donors
  - ➢ $n_s \downarrow$, $R_{on} \uparrow$ and $g_m \downarrow$ revert to virgin state: complete recovery

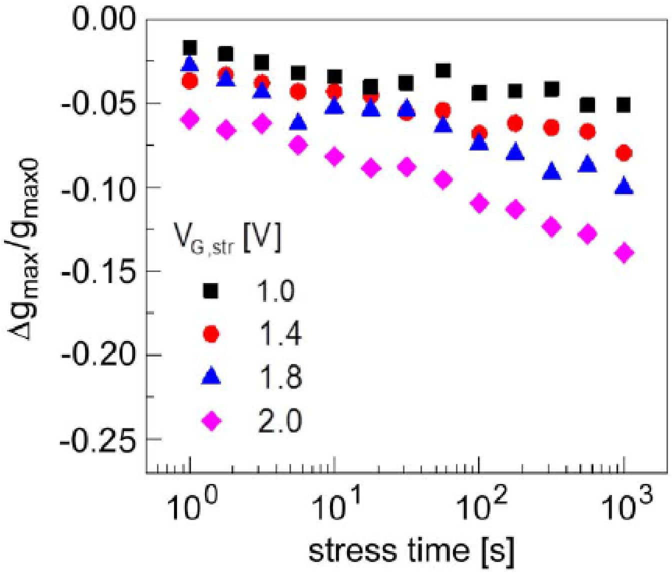
Forward Gate Stress

- Comparison with *Positive Bias Temperature Instability* (PBTI) study in other InGaAs MOSFETs:

This work



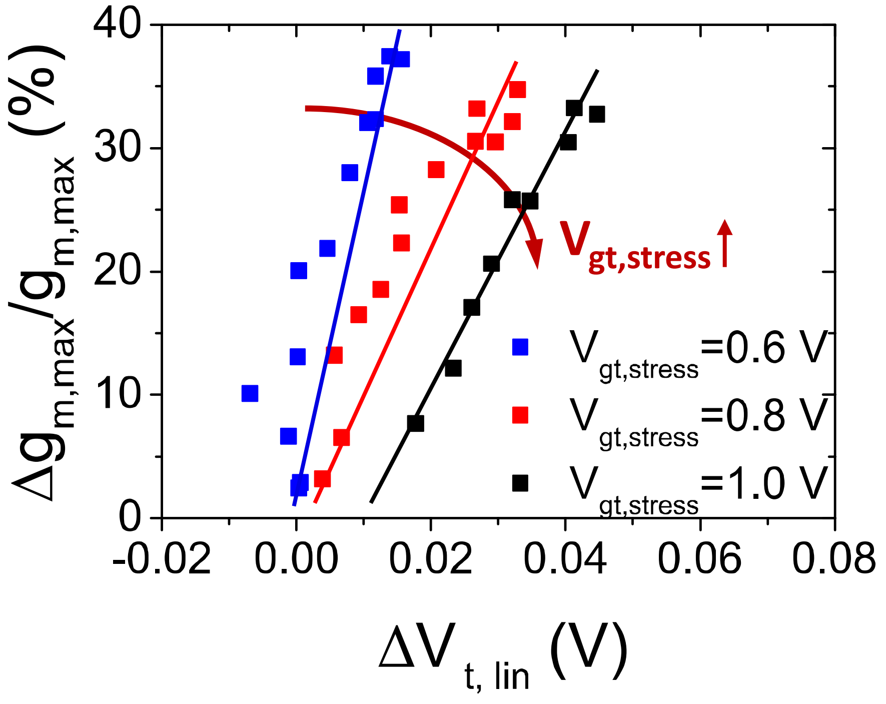
S. Deora et al, TED 2013



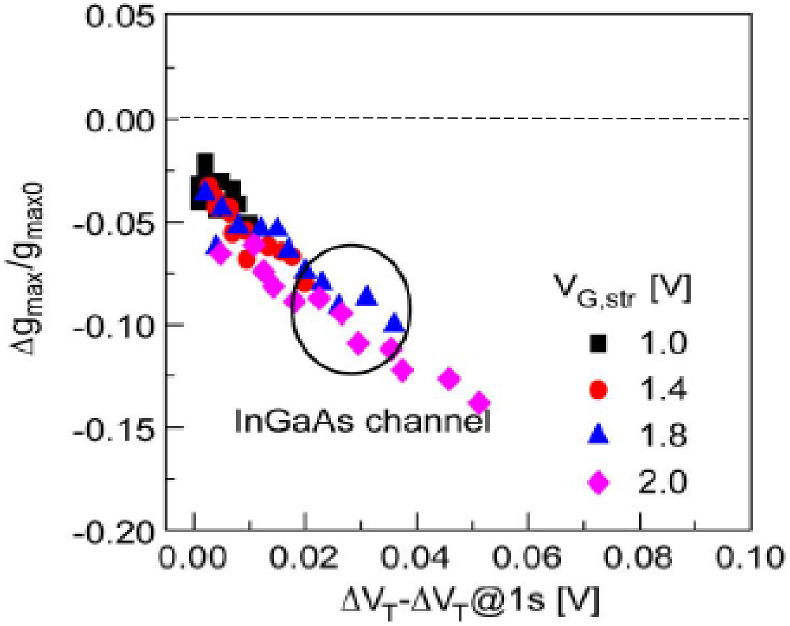
- This work: g_m↑ vs. PBTI: g_m↓
- This work: fast vs. PBTI: slow

Forward Gate Stress

- Positive gate voltage stress at different $V_{gt,stress}$



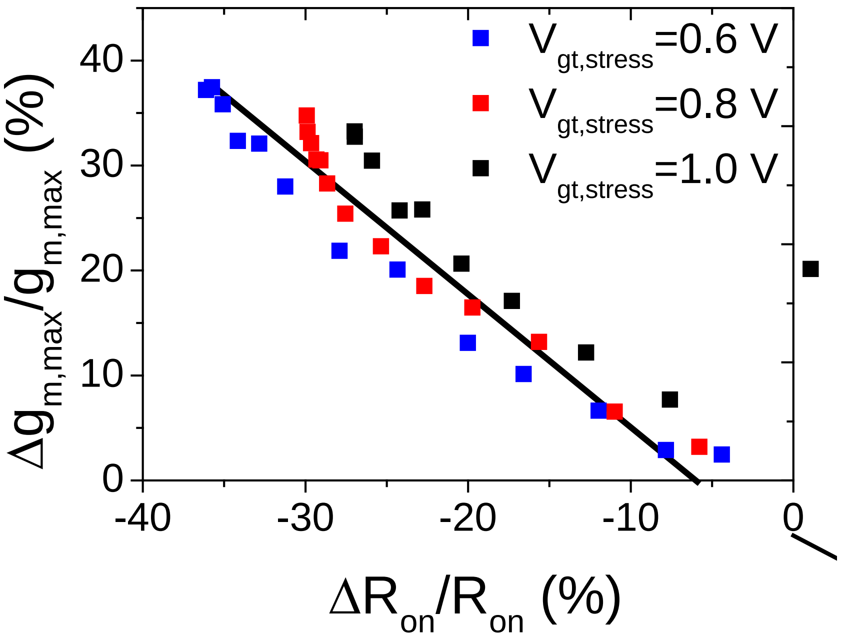
S. Deora et al, TED 2013



- $\Delta g_{m,max}$ - ΔV_{tlin} correlation inconsistent with established PBTI
- No universal relation between Δg_{max} and ΔV_{tlin}

Forward Gate Stress

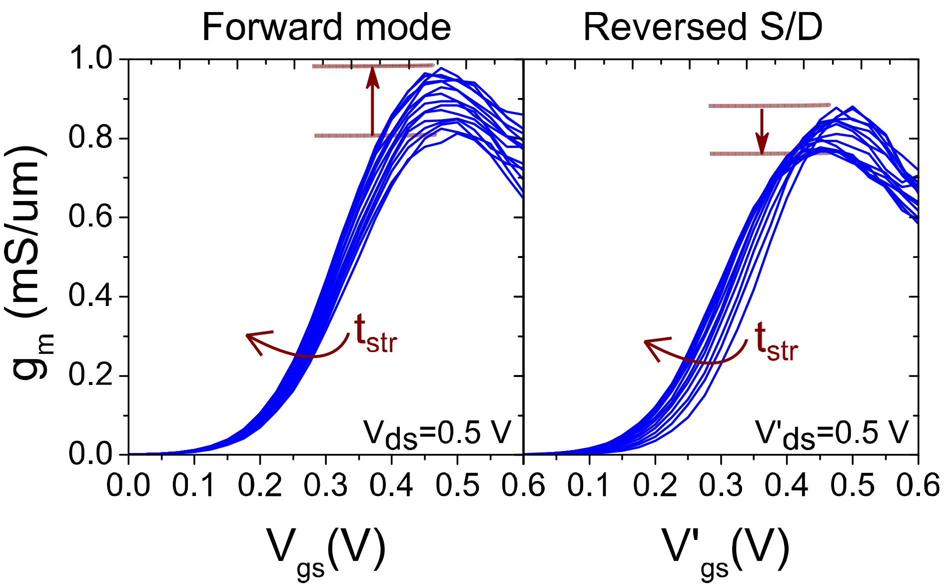
- Positive gate voltage stress at different $V_{gt,stress}$

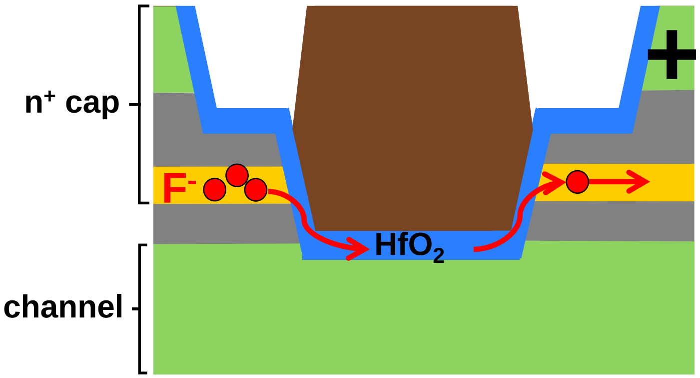


- Universal relation between Δg_{max} and ΔR_{on}
- Connection between g_m instability and extrinsic portion of the device

Off-State Stress

- Stress: V_{gt}=0 V, V_{ds}=0.7 V, 2 h, at RT



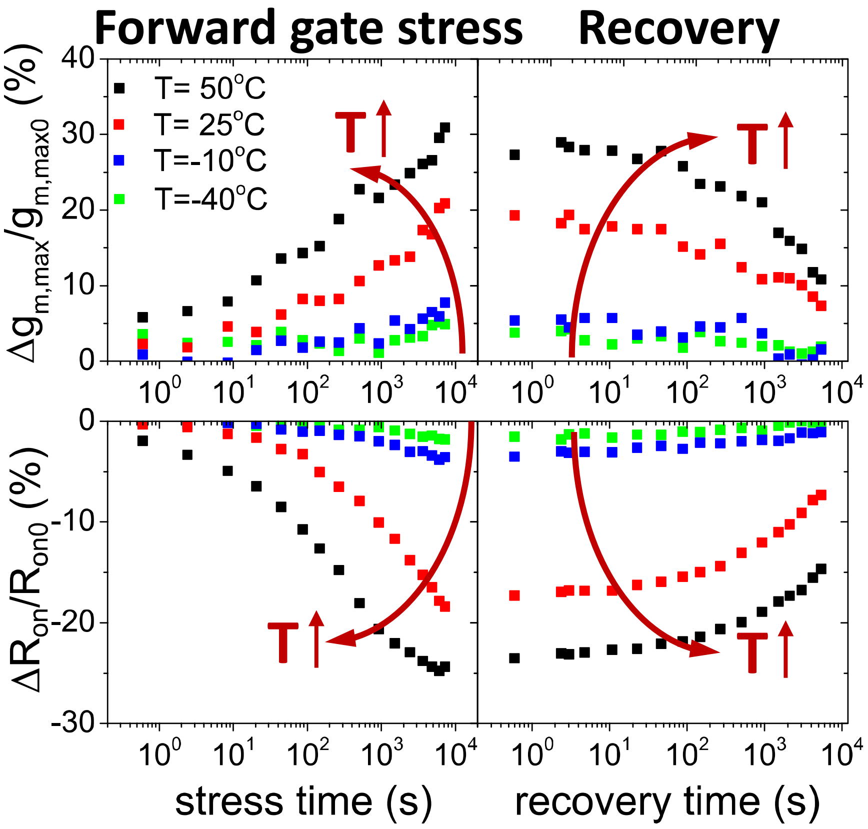


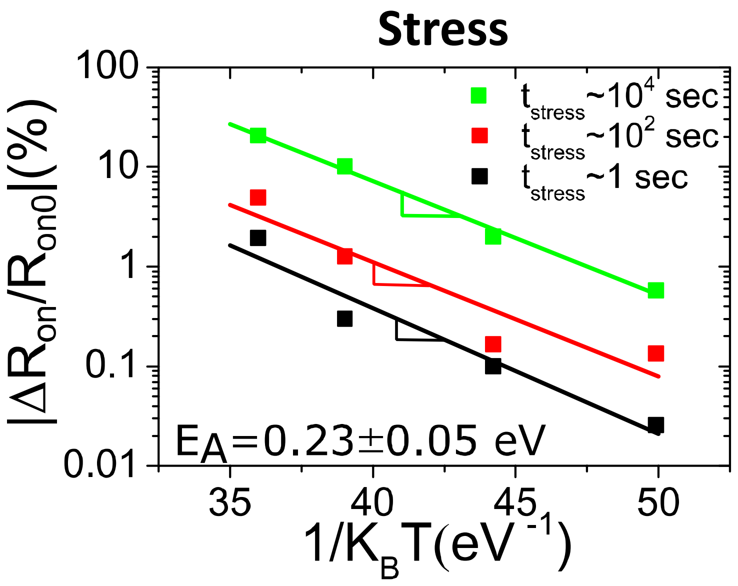
Off-state voltage stress
(V_{ds}>0 V)

- Lateral E-field sweeps F^- away from source and gate oxide towards drain
  - On source side: Si dopants reactivated, g_m↑ in forward mode
  - On drain side: Si dopants passivated, g_m↓ in reversed mode

Temperature Dependence

- Forward gate stress: V_{gt} =0.8 V, V_{ds}=0 V, 2 h, at various T
- Recovery: V_{gs} =0 V, V_{ds}=0 V, 1.5 h, at same stress T





- E_A=0.23±0.05 eV, consistent with estimated F-Si ionization energy (A. Taguchi et al, Phys. Rev. B 2000)

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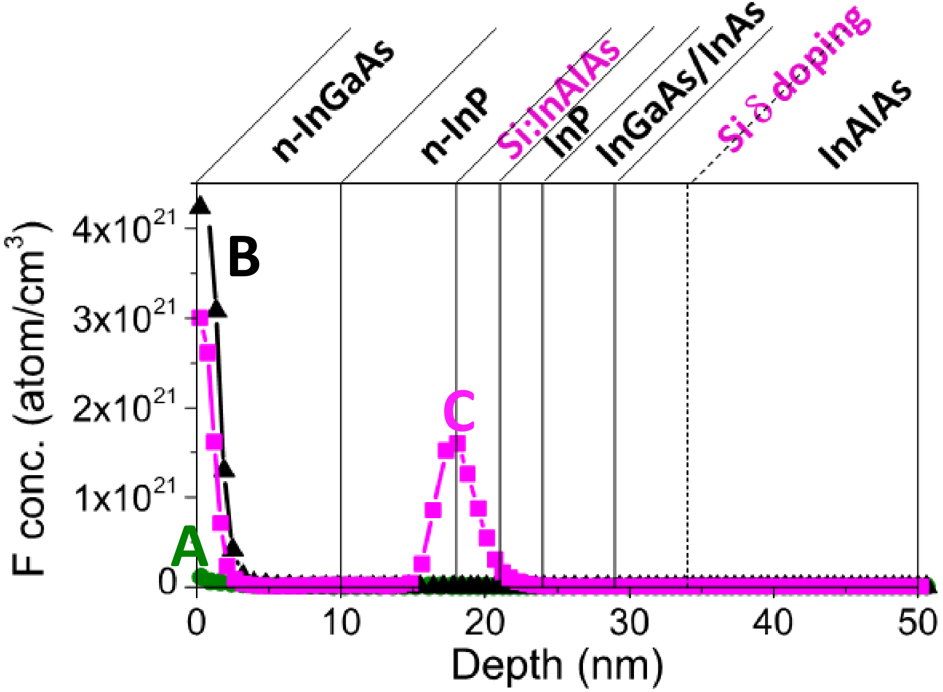
Independent Confirmation: SIMS

- 3 samples containing 3 nm-thick buried Si:InAlAs layer

Sample #	Process
A	never exposed to F
B	exposed to Mo sputtering and F-based RIE
C	Process of B + annealing at 350°C & 1 min

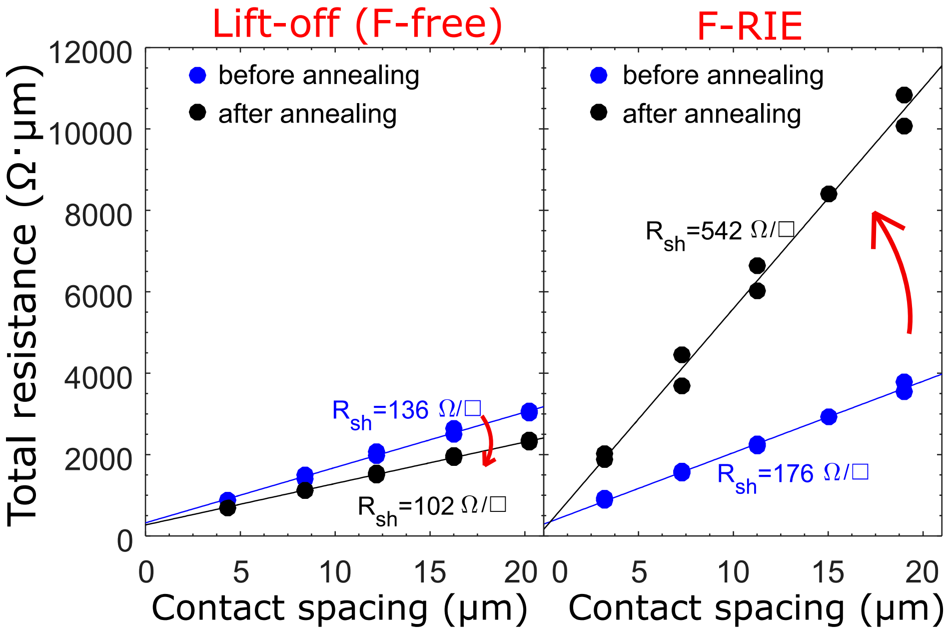


- Samples B and C show high surface concentration of F
- Sample C shows additional pile-up in Si:InAlAs layer
- Verifies F migration to Si:InAlAs in our structure

Independent Confirmation: TLM

- Sample with cap containing 3 nm-thick Si:InAlAs
- TLMs measured before and after annealing at 350°C for 1 min

Sample #	**Mo Contact Process**
A	lift-off (no exposure to F)
B	sputtered and etched by SF_6/O_2 RIE (as in MOSFET process)



- **F-free sample: annealing → R_{sh} ↓**
- **F-RIE sample: annealing → R_{sh} ↑ by 3X**
- Verifies F$^-$ induced donor passivation in our process

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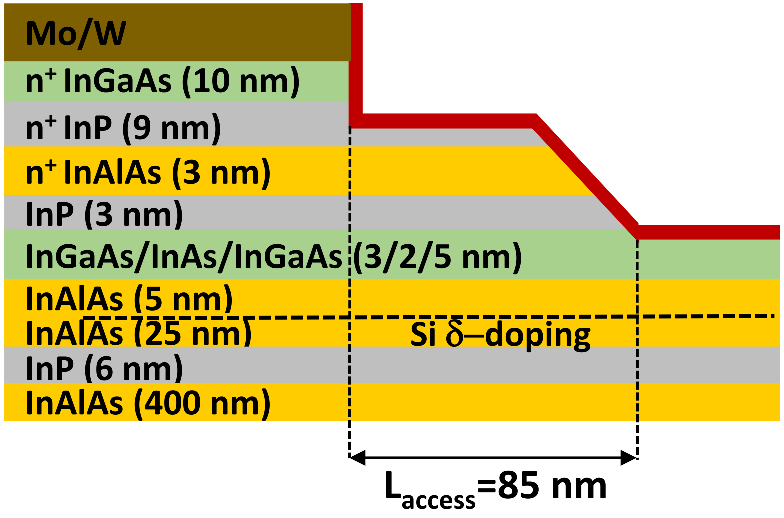
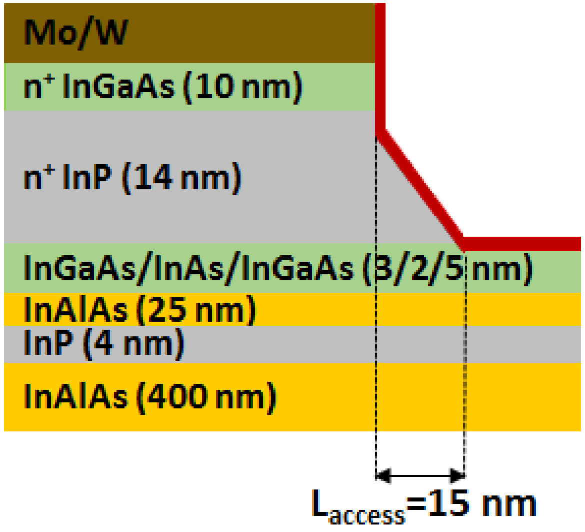
Mitigation: New MOSFET Structure

- Potential solution: **eliminate Si:InAlAs**
- New device structure: **use n-InP in access region**

Original device structure



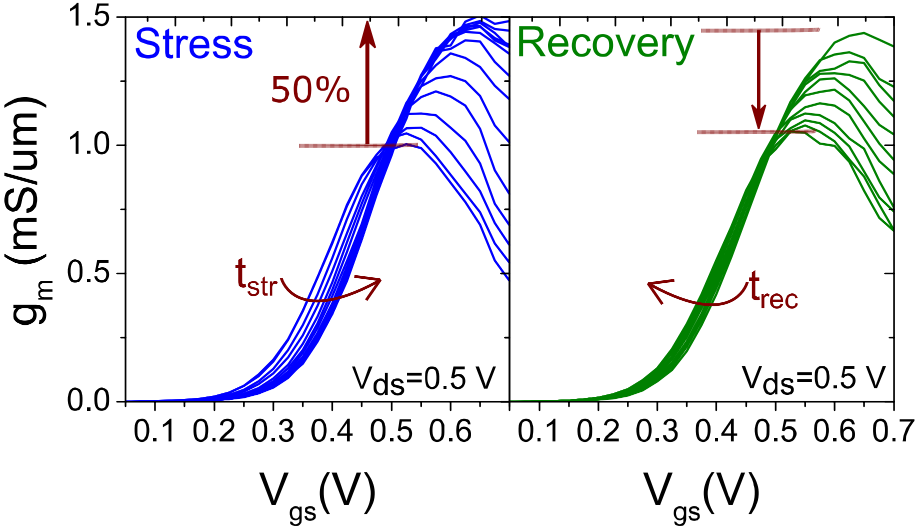
New device structure



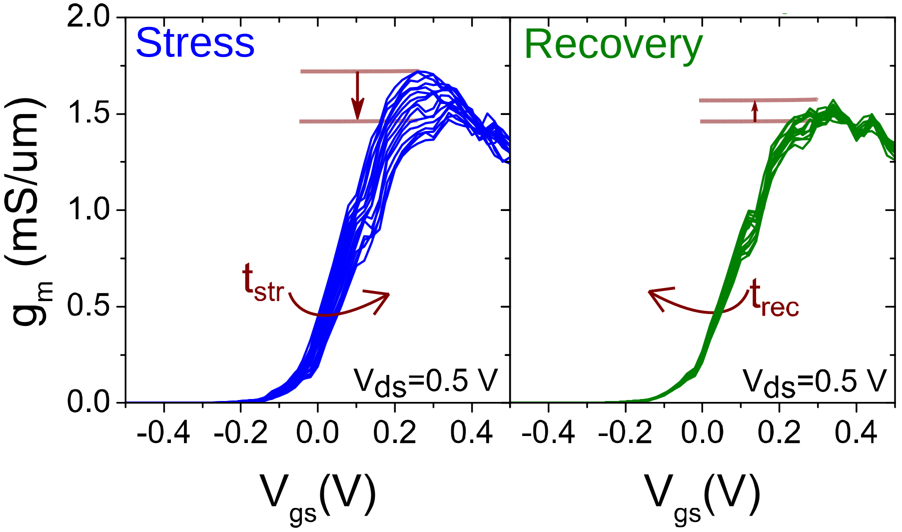
Improved Electrical Stability

- Response to forward gate stress (V_{gt}=0.8 V and V_{ds}=0 V)

Original Structure



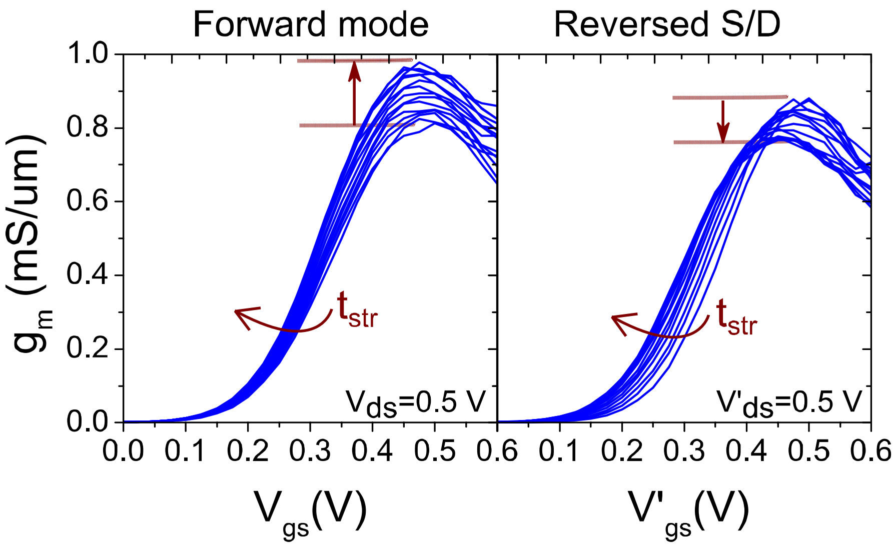
New Structure



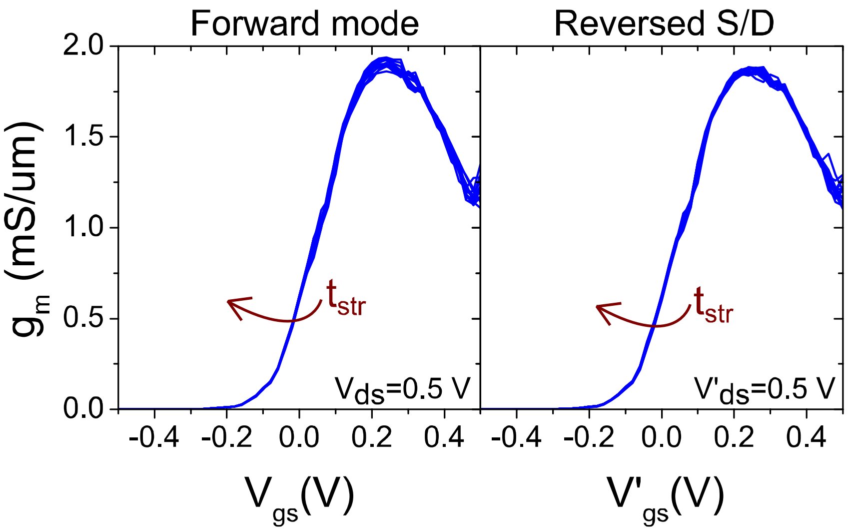
- New device: $g_{m,max}$ ↓ (up to 15%), small ΔV_t >0, classic PBTI behavior

Improved Electrical Stability

- Response to off-state stress (V_{gt}=0 V and V_{ds}=0.7 V)



Original Structure

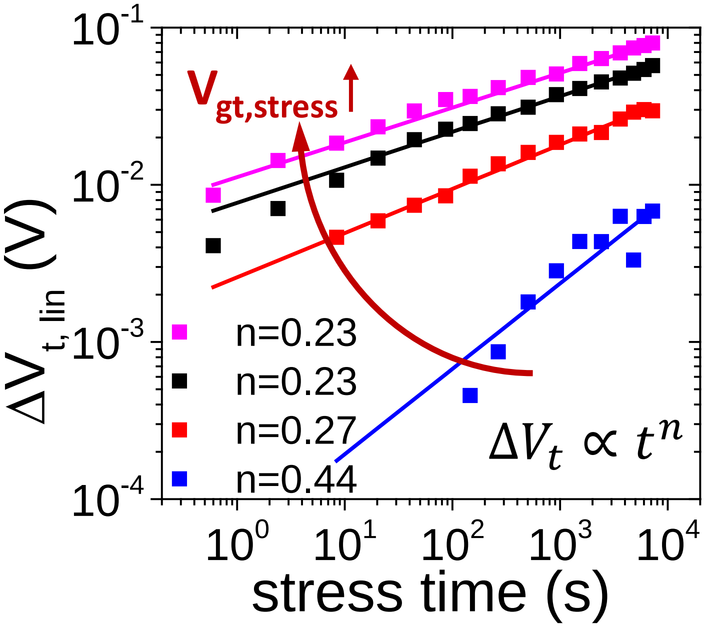


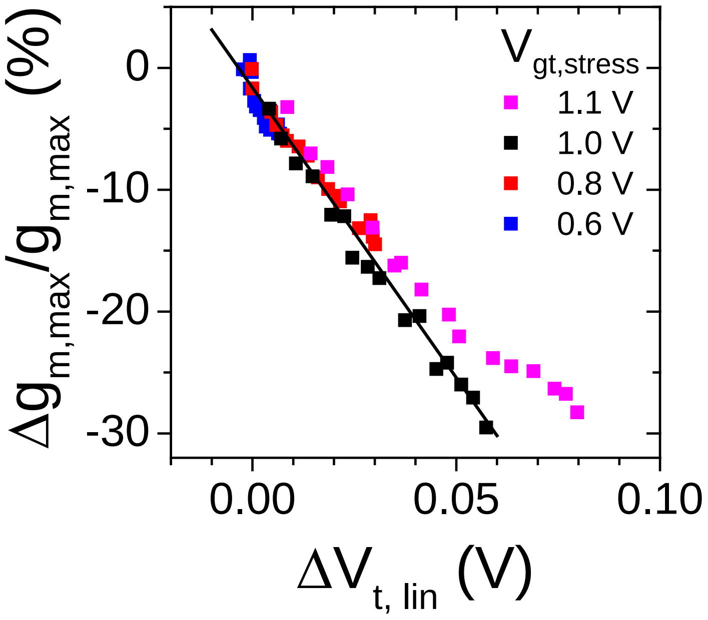
New Structure

- New device: minimal change

Classical PBTI Behavior

- Positive gate voltage stress at different $V_{gt,stress}$ at RT

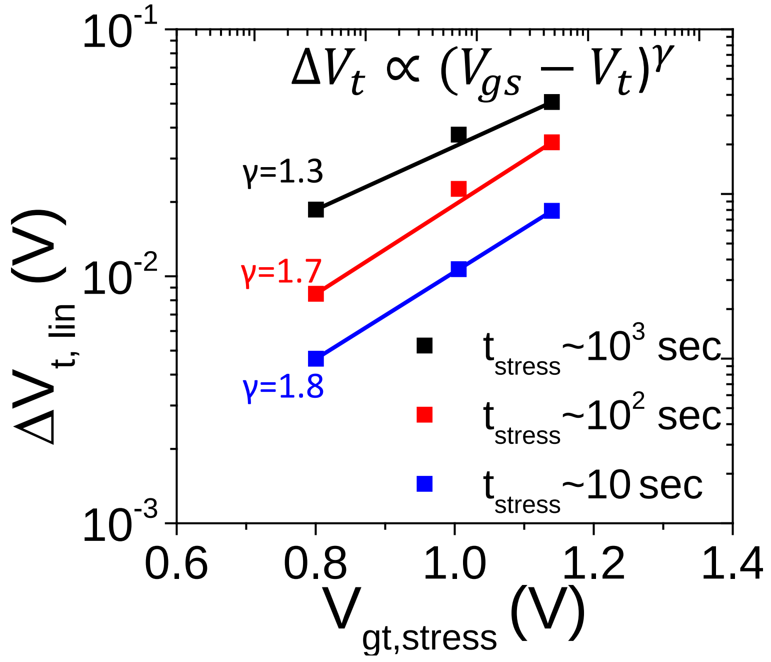




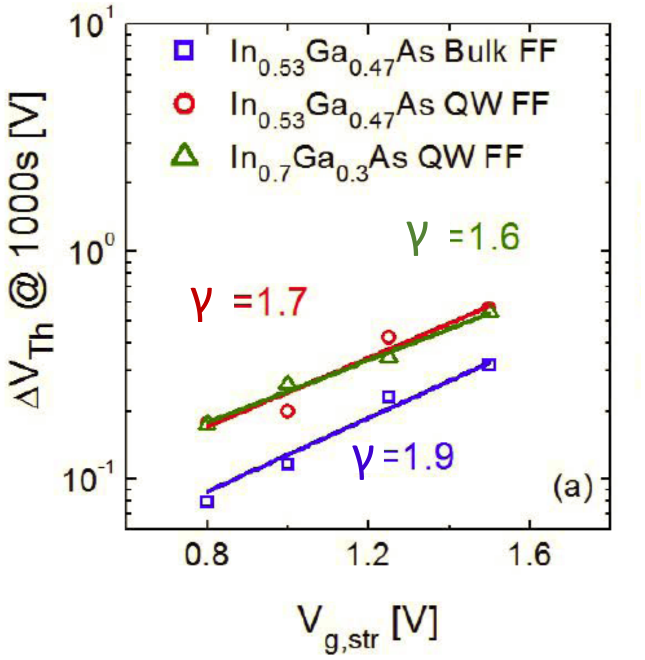
- $\Delta V_{t,lin}$ follows power law with time exponent n~0.23-0.44
- Strong correlation between Δg_{max} and $\Delta V_{t,lin}$ at different $V_{gt,stress}$
- Typical of PBTI

Classical PBTI Behavior

- Positive gate voltage stress at different $V_{gt,stress}$ at RT



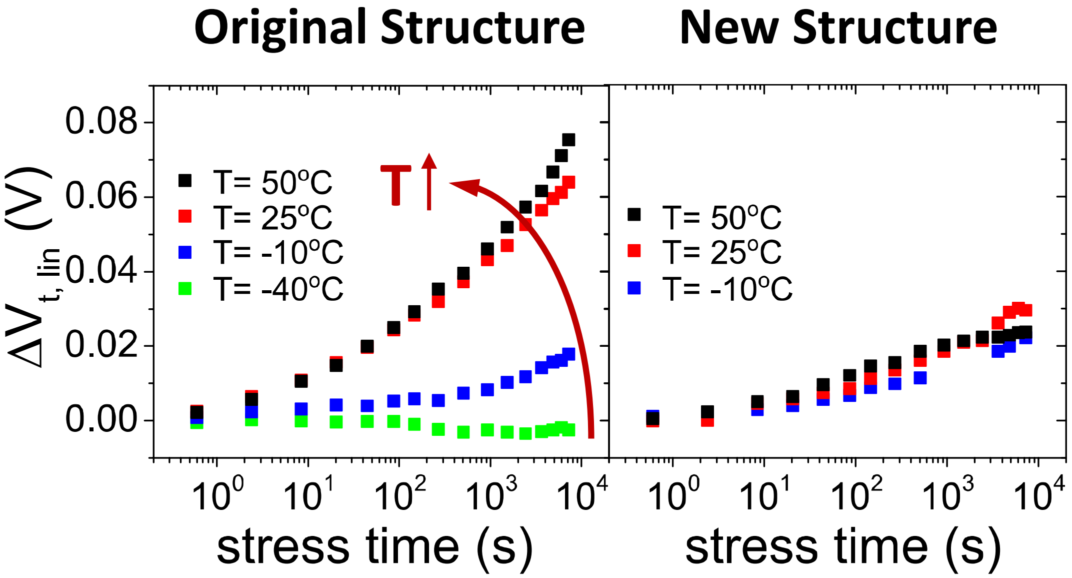
N. Agrawal et al, EDL 2015



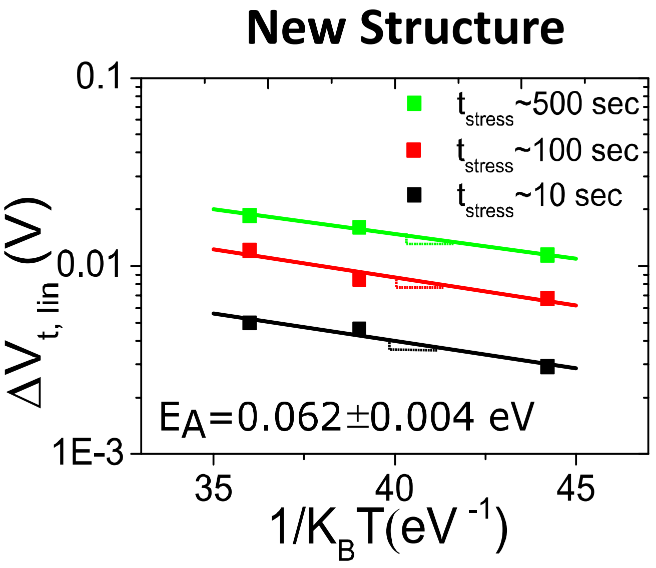
- Stress voltage exponent γ~1.3-1.8, similar to other studies in InGaAs MOSFETs PBTI

Weak Temperature Dependence

- Forward gate stress: V_{gt} =0.8 V, V_{ds}=0 V, 2 h, at different T



Original Structure **New Structure**

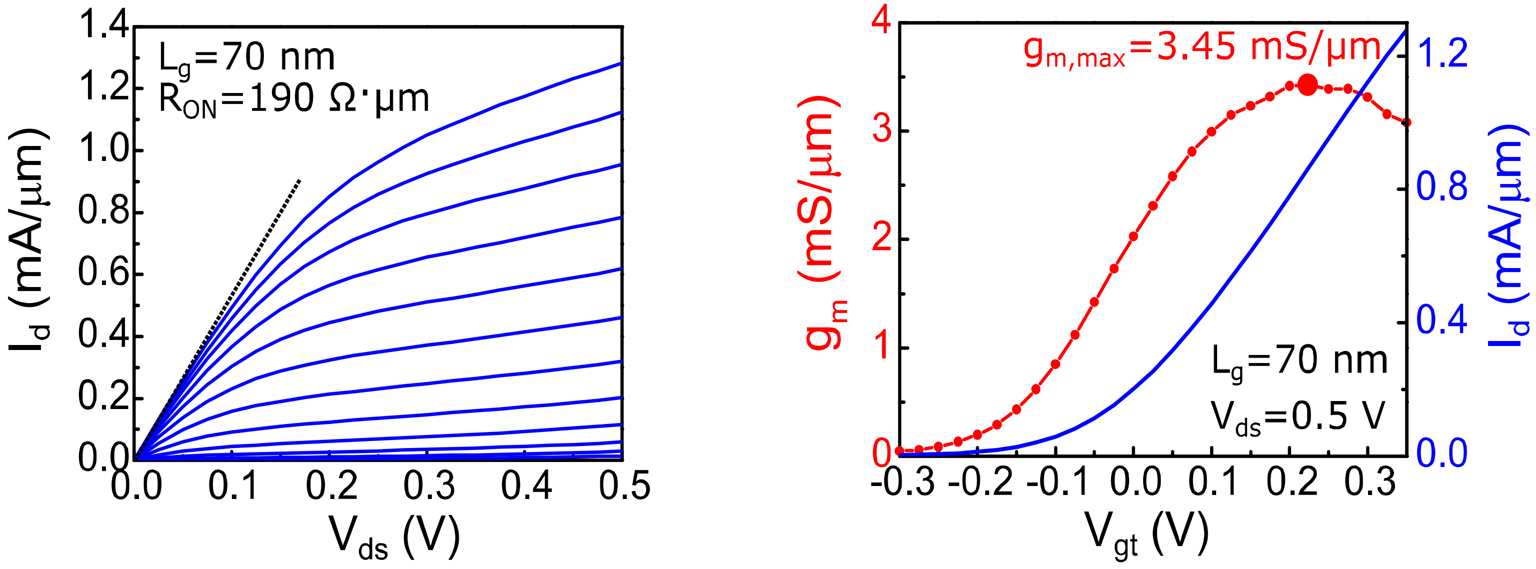


New Structure

- New structure: reduced V_t sensitivity with T
- Weak T dependence with E_A=0.062±0.004 eV
- Characteristic of border traps that communicate through tunneling

Record Performance

- Absence of Si:InAlAs mitigates F donor passivation → R_{on}↓ → g_m↑



J. Lin et al., EDL (2016)

- R_{on} = 190 Ω·μm
- $g_{m,max}$ = 3.45 mS/μm (new record for InGaAs FETs of any kind)

Conclusions

- Identified instability mechanism in self-aligned InGaAs MOSFETs caused by F^- migration and (de)-passivation of Si dopants in InAlAs
- Successfully mitigated problem by eliminating Si:InAlAs from device structure
- New device design achieved improved stability and record device performance

Thank you!